The Impact of Multiplexing on the Dynamic Requirements of Analog-to-Digital Converters

Tim J. Sobering, *Member, IEEE,* and R. Rex Kay

Abstract— **In data acquisition applications where the signals being digitized are produced in a time-division multiplexed system, the required dynamic performance of the analog-to-digital converter (ADC) is no longer bound by the conditions set forth in the Sampling Theorem. This results from the introduction of very high-frequency information by the multiplexing process which, while not necessarily containing information of interest, must be processed by the input circuitry of the ADC. In this situation, signal bandwidths and slew rates can greatly exceed those produced in a Nyquist limited system and can surpass the capability of the ADC, thus degrading overall system performance. This paper will examine two common multiplexing schemes and their impact on ADC dynamic requirements. First, we will examine a simple voltage multiplexing scheme typically found in state-of-health or data-logging applications and develop the necessary equations to show how the ADC dynamic requirements are affected. Then, the analysis will be extended to a multiplexed photodiode array readout to see how this application further challenges the dynamic performance of the ADC. Finally, the issues associated with developing dynamic test methodologies for assessing ADC performance in multiplexed systems will be discussed.**

I. Introduction

ANALOG-TO-DIGITAL converters (ADC's) are typically applied in one of three modes of operation, DC conversion, signal reconstruction, or time-division multiplexing. In the DC conversion mode, the ADC sees a stable voltage between samples, during sample acquisition, and during the conversion process. The second mode, signal reconstruction, requires that the conditions of the Nyquist Theorem be met so as to permit either estimation of the signal value between sample points, or accurate transformation of the signal information to the frequency domain. The final mode is time-multiplexed operation, which occurs whenever multiple signal sources are presented to a single ADC. This commonly occurs in state-of-heath or multichannel data-logging applications, but also less obviously in electronic imaging applications such as the readout of CCD or self-scanned (multiplexed) photodiode arrays. In this mode, the ADC sees a pseudo-DC input level during sample acquisition and conversion, but the signal can vary up to the full-scale level between conversions. Depending on the means of generating the multiplexed signals, the frequency content of the resulting waveform can greatly exceed the Nyquist frequency derived from the ADC sampling rate. This results from the presence of very high-frequency information which, while not necessarily containing information of interest, must be processed by the input circuitry of the ADC. If the ADC input circuit has an insufficient bandwidth or slew rate, system performance will be degraded. While the first two modes of operation fall within the scope of the conventional static and dynamic tests applied by manufacturers, the time-division multiplexing mode does not.

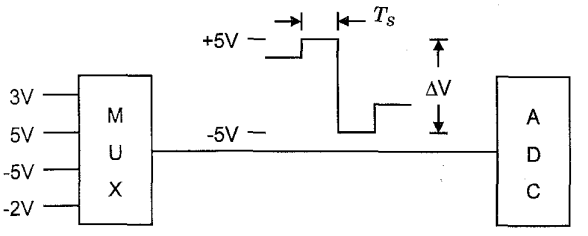

Fig. 1. Example of a multiplexed input signal.

II. Simple Multiplexed System Analysis

For the case of a simple multiplexed system, the analysis of the effects introduced by the multiplexing process is straightforward and can be accomplished by examining the transient signals produced when the multiplexer sequences between channels. Fig. 1 illustrates this configuration and shows the typical waveform produced. In reality, the input waveform will be slew rate and bandwidth limited due to the multiplexer "on" resistance and capacitive loading, but the primary limits will typically be due to the input circuitry of the ADC. If we assume a single-pole transfer function for the input stage of the ADC, the step response obtained for a worst-case (full-scale) change in the multiplexed voltage (ΔV) is given by

$$v_o(t) = \pm\Delta V(1 - e^{-2\pi\Delta f t}) \tag{1}$$

where Δf is the 3 dB bandwidth of the system. Examining the error term in (1) shows that for an ADC of resolution N, the bandwidth required for the input step to settle to within one-half of the least significant bit (LSB) in the sampling period T_s is given by

$$\Delta f \geq \frac{\ln(2^{N+1})}{2\pi T_s}. \tag{2}$$

Recalling that the Nyquist frequency f_N is related to the sampling period by

$$f_N = \frac{1}{2T_s} \tag{3}$$

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The authors are with Sandia National Laboratories, Albuquerque, NM 87185 USA.

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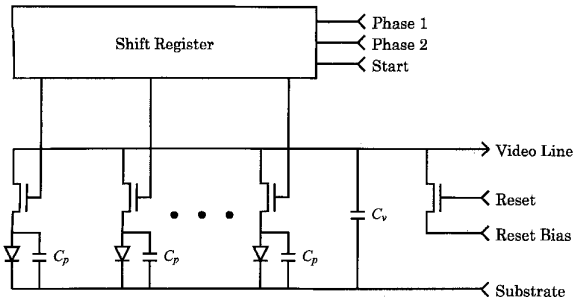

Fig. 2. Typical multiplexed photodiode array readout topology.

and using (3), (2) can be expressed as

$$\Delta f \geq \frac{\ln(2^{N+1})}{\pi} f_N. \tag{4}$$

Applying (4) illustrates that for an 8-bit ADC, a system bandwidth of nearly twice the Nyquist frequency is required for the signal to settle to the necessary accuracy. For 12-bit and 16-bit ADC's, this increases to 2.87 f_N and 3.75f_N, respectively.

Another parameter influenced by multiplexing is slew rate. In conventional dynamic testing, the worst case signal is a full-scale sinusoid near the Nyquist frequency. If we examine a sinusoid of frequency f_N and peak-to-peak amplitude of ΔV, the maximum rate of change of the signal is given by

$$\frac{dV}{dt}(\max) = \pi f_N \Delta V. \tag{5}$$

However, differentiating (1) and computing the maximum rate-of-change, using the bandwidth from (4) yields

$$\frac{dv_o(t)}{dt}(\max) = 2\ln(2^{N+1}) f_N \Delta V. \tag{6}$$

Comparing (5) and (6) shows that, due to the step nature of the input signal, multiplexing results in an increase in the maximum slew rate when contrasted with typical sinusoidal ADC test signals. In the above example, multiplexing results in the slew rate requirement increasing by a factor of 3.97 for an 8-bit ADC, 5.74 for a 12-bit ADC, and 7.5 for a 16-bit ADC.

The brief analysis above illustrates that the bandwidth and slew rate requirements for an ADC are significantly increased by operating in a multiplexed mode, and care should be taken in selecting a component for this application. The fact that the analysis neglects amplitude errors due to frequency response rolloff and the second-order effects in the input stages of the ADC does not invalidate the conclusion, since these effects serve only to exacerbate the situation, thus making the requirements more stringent.

III. Multiplexed Linear Array Analysis

The logical extension of the above analysis is to the situation in which only a fraction of the sampling period can be devoted to settling the input to the ADC. This occurs when the signals are being generated by a multiplexed photodiode array. This case also compounds the problem because, unlike the simple

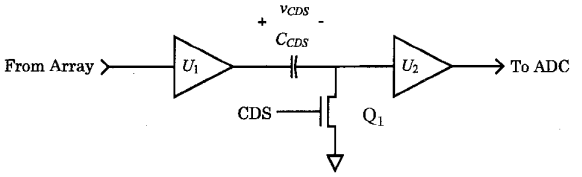

Fig. 3. Typical multiplexed photodiode array interface circuit.

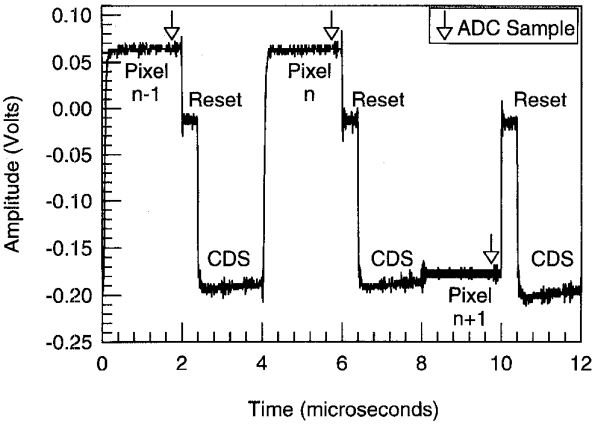

Fig. 4. Photodiode array preamplifier output.

multiplexing case, ADC's operated in this mode are typically operated at or near their maximum sampling rate, thus leaving no performance headroom. Fig. 2 shows a typical readout topology used in the Reticon© M-Series discrete photodiode array multiplexer.

Illumination of the photodiodes results in a charge being integrated onto the photodiode storage capacitors. The shift register serves to sequentially dump the individual integrated charge packets onto the shared video line. At the end of each readout period, the video line and photodiode storage capacitance are reset, and the process repeats for the next photodiode. Fig. 3 shows a typical interface circuit for converting the output charge packets to a voltage within the range of the ADC. The preamplifier, U_1, serves to buffer the high impedance of the video line and, along with the video line capacitance, to convert the stored photodiode charge to a voltage. The capacitor C_{CDS}, switch Q_1, and amplifier U_2 implement a correlated double sampling (CDS) circuit for the cancellation of kTC, or reset, noise. The output of U_2 is applied to the input of the ADC. Fig. 4 shows the signals produced at the output of the preamplifier, while Fig. 5 shows the signal applied to the input of the ADC.

It is important to note that the requirement for resetting the video line and allowing the voltage on the capacitor in the CDS circuit to settle results in, typically, no more than 50% of the sampling period being available for settling the input to the ADC. In addition, the contrast variations illustrated by the data shown in Figs. 4 and 5 result in a full-scale signal change during this fraction of the sampling period. Taking this into account in the analysis in Section II, the minimum bandwidth

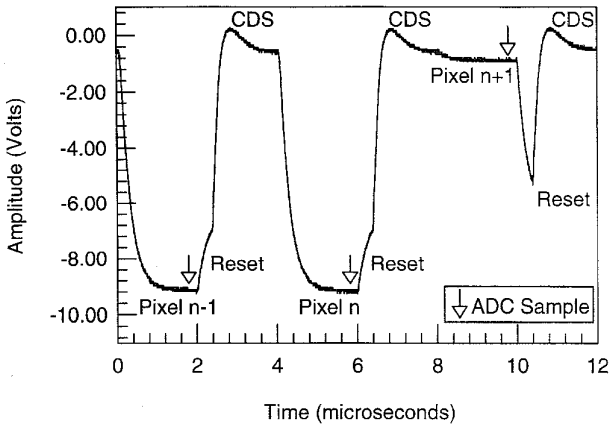

Fig. 5. Processed photodiode array signal.

TABLE I
BANDWIDTH AND SLEW RATE REQUIREMENTS SUMMARY

ADC Resolution (N)	Simple Multiplexing		Photodiode Readout	
	Minimum Bandwidth	Minimum Slew Rate	Minimum Bandwidth	Minimum Slew Rate
8	$1.99 f_N$	$12.5 f_N \Delta V$	$4.0 f_N$	$25.0 f_N \Delta V$
10	$2.43 f_N$	$15.3 f_N \Delta V$	$4.9 f_N$	$30.5 f_N \Delta V$
12	$2.87 f_N$	$18.0 f_N \Delta V$	$5.7 f_N$	$36.0 f_N \Delta V$
16	$3.75 f_N$	$23.6 f_N \Delta V$	$7.5 f_N$	$47.1 f_N \Delta V$

and slew rate requirements become

$$\Delta f = \frac{2 \ln (2^{N+1})}{\pi} f_N \tag{7}$$

$$\frac{dv_o(t)}{dt} (\max) = 4 \ln (2^{N+1}) f_N \Delta V. \tag{8}$$

As expected, the requirements are doubled from the simple time-division multiplexing case. Table I summarizes these results. Note that while one can argue that a sample-and-hold (S&H) can convert the signal in Fig. 5 to one equivalent to that produced by the simple multiplexing case, this simply shifts the performance requirements from the ADC input circuitry to the external S&H, and the argument still stands.

IV. DYNAMIC TESTING OF MULTIPLEXED ADC'S

There is a suite of test techniques, both static and dynamic, available for evaluating the performance of ADC's under various operating conditions. Static testing, which utilizes a near DC signal to stimulate an ADC, is only useful for evaluating ADC's which are to be operated in a DC conversion mode. In this mode, the major sources of error are nonideal offset and gain, which can be calibrated out, device feedback due to dynamic input impedance, and conversion process errors such as missing codes, integral nonlinearity (INL), and differential nonlinearity (DNL). Static testing will accurately measure these errors, but there may be little correlation to the performance of the device under dynamic conditions.

The majority of attention in the technical literature has been given to dynamic testing, which is directly applicable to testing ADC's used in the signal reconstruction mode. In this mode, the signal is changing, presumably up to but not exceeding the Nyquist rate, during the entire data acquisition and conversion process. Errors will result from all steps in the data acquisition and conversion process. Dynamic testing, which actually refers to a widely varied class of tests, is viewed as a means of fully characterizing the ADC. The three most common dynamic tests are the fast Fourier transform (FFT) test, the histogram test, and the sine wave curve fit [1], [2]. Other tests, such as beat frequency testing [3], could also be performed, but are less informative.

FFT testing involves applying a very low-noise, spectrally pure (harmonic distortion $<1/4$ LSB), near-full-scale sine wave to the device-under-test (DUT) and then computing the FFT from the data. The resulting spectrum is used to measure the dynamic integral nonlinearity and the signal-to-noise ratio (SNR) of the ADC. From the estimated SNR, the effective number of bits (ENOB) can be computed. One advantage of FFT testing is that it can be performed with a relatively small number of samples (nominally 1024), but several drawbacks do exist. First, FFT tests only exercise a small fraction of the codes on a high-resolution (12–16 bits) converter. Also, FFT testing lumps together system noise, DNL, and aperture uncertainty which cannot be separated using this technique. For this reason more rigorous tests have been developed.

The best test for measuring dynamic DNL is the histogram test. In this test, a low-noise, low-distortion sine wave is applied to the DUT. The amplitude of the sine wave must be sufficient to slightly overdrive the ADC. After sampling a large number of cycles, the histogram is formed using the number of occurrences versus output code. DNL, missing codes, gain errors, and offset errors can then be determined. The drawback to histogram testing is that a large number of samples (and potentially a long period of time) are required to obtain an accurate measurement. Also, for low sampling rates, temporal and thermal variations in the test equipment and DUT can be a problem.

The final test mentioned is the sine wave curve fit. This test yields the total rms error in the converter which is used in the calculation of ENOB. For this test, a spectrally pure low-noise sinusoid (noise and harmonics $\ll 1$ LSB of the DUT) is applied to the DUT. The amplitude of the signal is significant. Manufacturers use anything from 1/4 full-scale to full-scale signals in their testing. The most demanding tests use full-scale signals, although 90% full-scale is becoming the standard since clipping caused by amplitude errors can severely skew test results. Once the samples are acquired, an ideal sinewave is fit to the data using least-squared error minimization techniques. The rms error between the actual sine wave and the ideal sine wave is then computed and compared to the rms error of an ideal quantizer of the same resolution as the DUT. This comparison yields ENOB. ENOB is defined as the number of bits of resolution required for an ideal ADC to exhibit an rms quantization error equal to the total rms error from all sources in the ADC under test. ENOB is becoming the standard by which ADC's and waveform recorders are judged. However, the drawback to this figure of merit is that it rolls all error sources together [4], an artifact of which is that devices with identical ENOB numbers can respond differently to the same input signal.

The above dynamic tests will reveal a great deal of information about the DUT, but will not accurately measure the performance of a device operated in time-division multiplexing mode. What is unique about this mode of operation is that the front-end amplifiers and S&H must track signals well in excess of the Nyquist frequency and have a fast enough settling time to permit an accurate conversion. This is contrary to the typical approach taken by manufacturers, who often do not specify converter input bandwidth or refer to the minimum input bandwidth as being "Nyquist." While this is acceptable for frequency-domain applications, *conventional dynamic testing assumes that signals above the Nyquist frequency have been eliminated,* which is not the case in a time-division multiplexing mode of operation. In order to predict device performance in this case, a test methodology must be developed that evaluates the input amplifier and S&H bandwidth, slew rates and stability. The only test that comes close to this is the envelope test [1]. The envelope test digitizes a full-scale sinusoid with a frequency slightly offset from the Nyquist frequency. The resulting samples will show large amplitude variations sample-to-sample as the positive and negative extremes of the sinusoid are alternately sampled. The envelope test is the most stringent test of settling times for an ADC, and it will produce the full-scale amplitude changes observed in the simple multiplexing case. However, it falls short of emulating the high-frequency content and settling time restrictions present when sampling the output of a multiplexed photodiode array.

The dynamic tests described above were designed with specific applications in mind, namely signal reconstruction and frequency-domain transformation. What is required for testing ADC's used in electronic imaging applications is to re-examine the important characteristics of the signals produced and to design a dynamic test for that purpose. Electronic imaging differs from signal reconstruction applications in that it is strictly a time-domain data acquisition application. As such, it is difficult to interpret many of the commonly optimized performance specifications, such as harmonic distortion, in predicting imaging system performance. In imaging applications, the data acquisition system must 1) not introduce discontinuities where none exist, and 2) preserve the discontinuities (edges or contrast) present in the scene [5]. The first requirement is a measure of the DNL of the ADC and is important in applications where image quality is required, such as when the human eye is viewing the electronic image. Because the eye has excellent edge detection capability, the second requirement, which relates to the step response of the ADC, is frequently ignored. However, for applications such as machine vision or imaging radiometry, the accurate preservation of scene contrast or the absolute measurement of the radiance seen by each pixel is important.

In [5], Sabolis identifies DNL as the "single most important" specification for ADC's used in imaging applications and briefly discusses the importance of the full-scale step response. The problem is that in determining DNL, manufacturers typically rely on the histogram test, which neglects the differences between conventional dynamic testing and the more stringent requirements faced when interfacing to a multiplexed photodiode array. Sabolis also suggests a test for full-scale step response that is similar to the envelope test and which suffers from the same limitations when applied to electronic imaging applications. What is needed is a dynamic test which simulates the multiplexed signals described above and simultaneously evaluates DNL and step response. This can be accomplished by extending the concept of the envelope test to signals well in excess of the Nyquist frequency. The authors would like to propose a "contrast" dynamic test in which a variable-amplitude square wave is applied to the ADC. The signal would be generated using a digital-to-analog converter (DAC) with at least two bits greater resolution than the ADC, and the peak amplitude of the square wave would be increased (or decreased) by one least significant bit (LSB) for each sample. Also, the phase of the DAC output and the ADC sample clock would be variable to simulate varying fractions of the sample period being available for settling. Nominally, a 90° phase shift would be used. Such a signal is illustrated in Fig. 6.

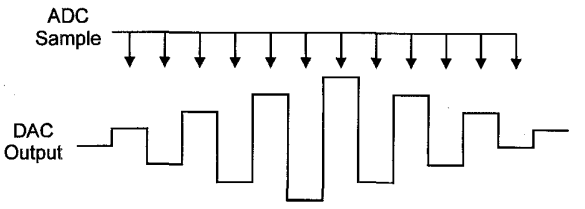

Fig. 6. Example of a "contrast test" using a 3-bit DAC.

The input data to the DAC would be compared to the ADC output data to determine DNL and to evaluate the incremental step response. The same test setup could be used to provide a precise ramp input to measure DNL and missing codes under less stringent conditions and to see how the performance degrades as a function of scene contrast. The validity of this approach will be studied by the authors in the future.

V. Conclusions

When applying ADC's in a time-division multiplexing mode, one needs to take into account the enhanced bandwidth and slew rate requirements that this type of operation places on the converter. Many of the conventional dynamic tests are oriented toward signal reconstruction or frequency-domain applications and are not sufficiently stringent to accurately predict the performance of a converter operated in this mode. Time-division multiplexing needs to be examined from a time-domain viewpoint, and new test methodologies, such as the contrast test, need to be perfected for these applications.

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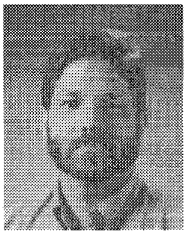

Tim. J. Sobering (S'81–M'82) was born in Devils Lake, ND, on August 8, 1960. He received the B.S. and M.S. degrees in electrical engineering from Kansas State University, Manhattan, in 1982 and 1984, respectively. He wrote his Master's thesis on the design of low-power, high-resolution analog-to-digital conversion systems.

In 1984, he joined the Sandia National Laboratories, Albuquerque, NM, working on the development of light-weight, low-power, "smart" sensor systems for intrusion detection. He is currently a Senior Member of the Technical Staff in the Sensors and Electronics Department 5722 at Sandia National Laboratories and is involved in the development of active and passive remote sensing technology for aircraft- and space-based systems.

R. Rex Kay received the B.S. and M.S. degrees in electrical engineering from the University of New Mexico, Albuquerque, in 1982 and 1983, respectively. Areas of specialized study were analog circuit design and microelectronics design.

Since 1983, he has been with Sandia National Laboratories, Albuquerque, NM. He is currently a Senior Member of the Technical Staff in the Sensors and Electronics Department 5722 where he has worked on a variety of space-based visible and infrared remote sensing systems.