# Power-Switched Sample-and-Hold Provides Accura Analog Inputs for ADC in Low-Power System

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*Abstract*—**This paper describes the design of a low-power, two-channel, 12-bit, data acquisition system with a conversion rate of 240 samples per second on each of the two input channels. Power switching the sample-and-hold module resulted in a power reduction of 140 mW compared with a continuously powered system. The total power consumption for the system was 102 mW. Preliminary information is given about the warm-up characteristics of a variety of operational amplifiers and a commercial sample-and-hold module; this is not available in the standard data books.**

## I. Introduction

An important requirement for a portable data acquisition system is that the power dissipation should be as small as possible in order to reduce battery size and weight and to obtain an extended operating life. Standard methods of reducing power dissipation include the use of CMOS devices, the use of the lowest possible clock frequency, and turning off any high-power modules when they are not in use. With this power-switched low duty-cycle operation, the following sequence is continually repeated:

a) turn power on;
b) wait for circuit to warm up and stabilize;
c) acquire data; and
d) turn power off.

Hence, the average power dissipation is given by

$$P_{\text{average}} = \frac{P_{\text{idle}} \cdot T_{\text{idle}} + P_{\text{warm-up}} \cdot T_{\text{warm-up}} + P_{\text{sample}} \cdot T_{\text{sample}}}{T_{\text{cycle}}}$$

where

$$T_{\text{cycle}} = T_{\text{sample}} + T_{\text{warm-up}} + T_{\text{idle}}.$$

When bipolar analog modules forming part of a data acquisition system are power switched, the warm-up behavior is critically important since failure to reach a steady-state condition during the measurement period will result in erroneous data. Since analog circuit modules are not normally operated in a power-switched mode, information is not available on warm-up characteristics. This paper presents some preliminary measurements of the warm-up characteristics of sample OP-01, OP-07, OP-20, LM741, LF351, LF356, and TL061 operational amplifiers, and the Analog Device AD583 sample-and-hold. These measurements were in turn used to design a power-switched, 12-bit, dual-channel data acquisition system with a total power dissipation of 102 mW [1].

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## II. Power Switching

Power switching is not a new concept; devices and commercial products such as calculators and instruments already exist on the market which go into a quiescent mode when not in use, consuming only a few hundred microwatts of power. Power switching devices that are not internally designed for such use, however, introduce several problems for the designer [2], [3]. First, a low-power method of switching the device must be determined, or the advantages of power switching are lost. Second, all of the inputs to the device must be disconnected before the power is switched off in order to prevent damage to the device. Also, substantial noise can be introduced on the analog signal and ground lines by the switching action, so the effect of this noise on the other parts of the system must be determined and steps taken to eliminate it if necessary. Finally, the "warm-up" time for each switched device must be measured and included in the ON time.

The method used to switch the power to a device depends on the supply current the device requires and the switching frequency. In our first attempt to power switch devices, bipolar junction transistors were used as switches but the control voltages were not easily generated and the circuitry consumed too much power. The second approach used opto-couplers to do the switching. This corrected the control voltage problem, but the opto-couplers ended up consuming more power than the device being switched. The eventual solution to the problem was to use overvoltage-protected analog switches, such as the Siliconix DG211CJ, to do the power switching. The DG211 is a quad CMOS SPST analog switch which consumes 20 mW of power per package. Each switch is capable of handling 20 mA of current continuously, and up to 70-mA peak current. The DG211 also uses standard 0–5-V CMOS

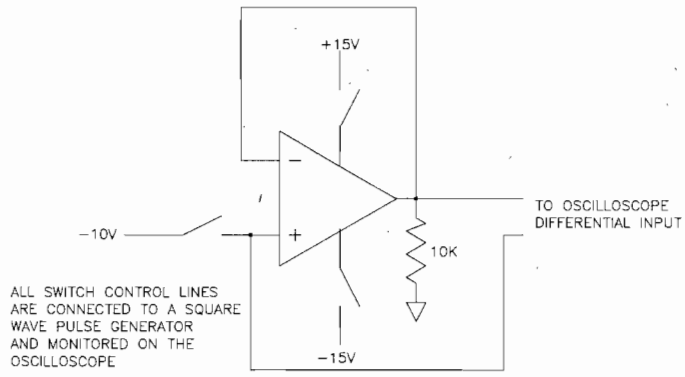


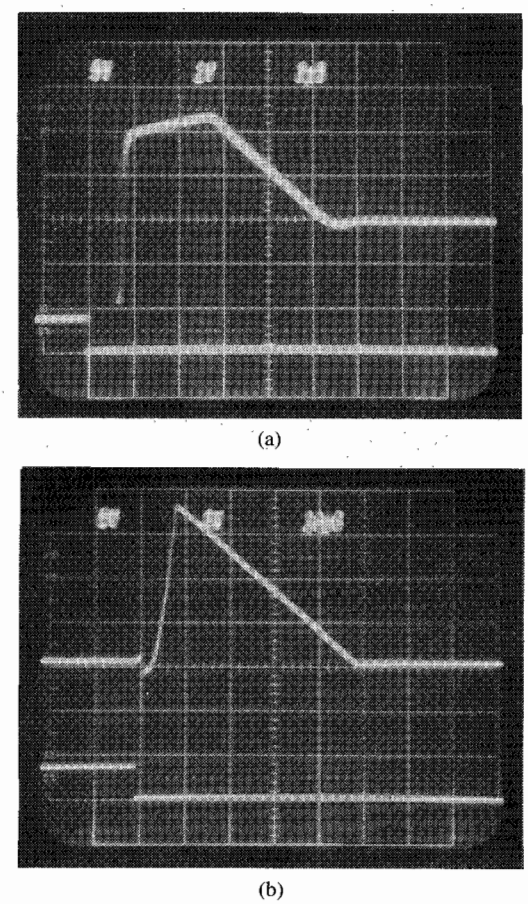

Fig. 1. Warm-up time test circuit for operational amplifiers.

logic levels, so interfacing to the control logic is simplified. The DG211 can also be used to switch the inputs to a device into a high-impedance state while the power is off, thus protecting the power-switched device from damage. Also, since the DG211 has a low ON resistance and was designed for low transient switching, such as that required for a sample-and-hold, the switching action will introduce a minimal amount of noise into the system.

## III. Warm-Up Times for Operational Amplifiers

The "warm-up" time for a system is defined as the amount of time from power-up to the point where the device can be effectively used to perform its function to some specified accuracy, which is determined by the requirements of the system. The warm-up times for several operational amplifiers were measured in an effort to establish a relationship between warm-up time and amplifier slew rate. When performing these tests, the input to the operational amplifier was connected to a −10-V source. A negative input voltage was used because the slew rate for a negative signal is typically less than or equal to the slew rate for a positive signal and thus would yield the worst-case warm-up time.

The circuit used to measure warm-up time is shown in Fig. 1. The amplifier under test was connected in a unity-gain configuration with a 10-kΩ load. The power switching was performed using Siliconix DG211 switches, which were also used to switch the input signal to the device. The input and output to the operational amplifier were connected to the differential input of an oscilloscope. The control signal to the switch was also monitored on the oscilloscope. Representative samples of the results obtained are shown in Fig. 2. The warm-up time was taken to be the amount of time for the error signal, given by the difference between the input and output voltages, to stabilize at or near 0 V. As can be seen in the photographs (Fig. 2), the OP-07, which has a typical slew rate of 0.3 V/μs, took 50 μs to stabilize, while the OP-01, which has a higher typical slew rate of 18 V/μs, took 12 μs. These results imply that the warm-up time for a device is directly related to the slew rate of the amplifiers making up the device. In general, this comparison is valid, however, there are other factors involved, the most important of which is the internal design of the amplifier. A more detailed summary of the results of the warm-up time tests is shown in Fig. 3.



(a)

(b)

Fig. 2. Warm-up time measurements for (a) OP-01, and (b) OP-07.

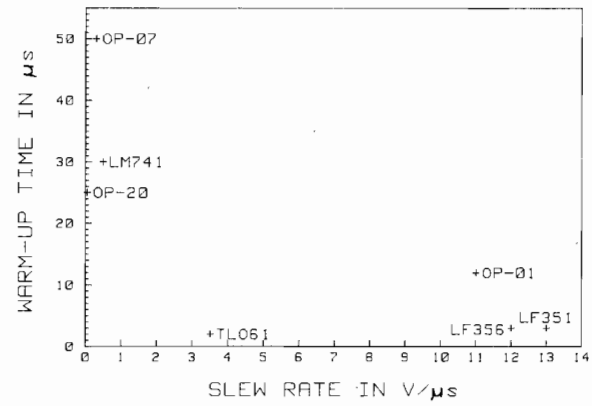



Fig. 3. Warm-up time test results.

## IV. Warm-Up Time for the Sample-and-Hold

The power switching of analog devices realizes the greatest advantage when applied to devices having short warm-up times. This allows the designer to use fast, high-performance devices in place of the low-power devices which are often too slow for a given application, and also minimize the ON time in a system, providing a greater reduction in the power consumption. In the case of the

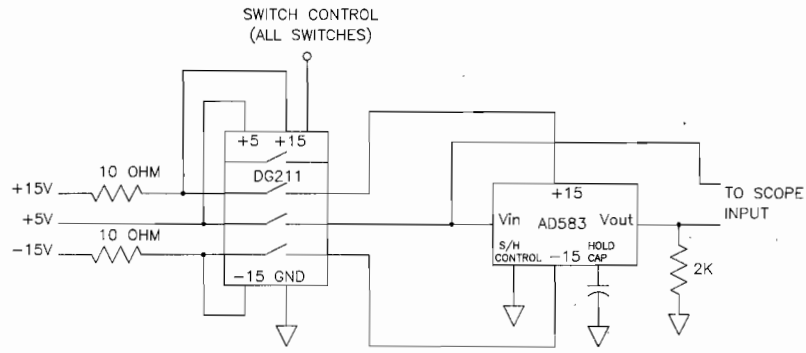



Fig. 4. AD583 test circuit.

12-bit system described in this paper, a sample-and-hold with a short acquisition time was required in order to minimize the phase difference between the samples obtained from each channel. The Analog Device AD583 IC sample-and-hold was chosen because of its low acquisition time (4 $\mu$s) and high slew rate (5 V/$\mu$s). However, according to the data sheet, the power consumption of the AD583 is in the 75–150-mW range. Thus it was decided to attempt to power switch the device and measure the amount of degradation in its response.

First, the circuit shown in Fig. 4 was built and used to measure the warm-up time and the power consumption of the switched system. With the DG211 control inputs grounded (switches closed), the supply currents through the 10-$\Omega$ sense resistors were measured to be 6.16 mA at +15 V and 2.32 mA at −15 V, corresponding to a power dissipation of 127.2 mW. In order to determine the power consumption of the switched system, the voltage across the 10-$\Omega$ sense resistors was monitored using the differential input on an oscilloscope. The results for the positive supply show that there is a brief (3 $\mu$s) 36-mA pulse when the switch closes, followed by a constant dc current of 6.6 mA. Similar results were obtained using the sense resistor in the negative supply lead. As a result, if the turn-on spike is neglected, the power dissipation of the switched device is equivalent to its continuous power dissipation multiplied by the fraction of time that the device is ON in one cycle. Such an estimation is quite accurate, especially if the duration of the turn-on spike is very short in comparison to the switching period. Naturally, as in the continuous operation case, the power consumption of the switched device will depend on the output load impedance, input voltage, etc.

After the feasibility of power switching the AD583 had been demonstrated, the final parameter to be measured was the warm-up time necessary for accurate operation. Using the same circuit as shown in Fig. 4 except with a −10-V input, the warm-up time was measured in a manner similar to that used for the operational amplifiers mentioned in Section III. However, in this case, it was realized that the warm-up time would be a function of the value of hold capacitor used, so measurements were made with an increasing series of capacitor values. It was found that for a holding capacitance of 0.0047 $\mu$F, a warm-up time of 90 $\mu$s is required. Capacitor values of 0.01 and 0.033 $\mu$F resulted in warm-up times of 130 and 180 $\mu$s, respectively. Obviously this result is not unexpected, since the hold capacitor acts as a load on the output of the first operational amplifier in the sample-and-hold and would act to slow down the response of the amplifier.

The final step was to measure the overall effect of power switching the sample-and-hold in the system. This will be discussed in the next section.

## V. Design of the 12-Bit System

Since the requirements for the operation of the power-switched sample and hold were known, the next step was to determine which ADC to use. It was decided that the Datel-Intersil ADC-HC12B 12-bit successive approximation ADC be used for the following reasons. First, the ADC-HC12B can be operated from a single positive supply voltage. Second, the ADC-HC12B is a complete ADC requiring only a few external resistors for offset and gain adjustments. Third, and most importantly, the ADC-HC12B is a hybrid integrated circuit fabricated using CMOS technology, noted for very low power consumption. Operating in the special low-power interrupt mode, the resulting power dissipation of the ADC-HC12B at a conversion rate of 480 conversions per second (240 conversions per second on two channels) is approximately 30 mW.

The disadvantage of such a long conversion time is that the sample-and-hold would have to be ON for 800 $\mu$s (two conversions), plus a warm-up time and a second acquisition time, or approximately 950 $\mu$s. Also, using the sample-and-hold in this fashion eliminates the benefit gained from having a fast acquisition time to reduce the phase error between the samples from the two channels. To correct this situation, the AD583 was used in conjunction with two low-speed "slave" sample-and-holds constructed using OP-20's, as shown in Fig. 5. Using this configuration, the AD583 can be turned on, allowed to warm up, take two fast samples, transfer them to the slave sample-and-holds, and then be turned off. The slave sample-and-holds, which are continuously powered, use only 5.5 mW of power. The slave sample-and-holds, however, are very slow to respond due to the low slew rate of the OP-20's. As a result, a delay of 200 $\mu$s, between the time

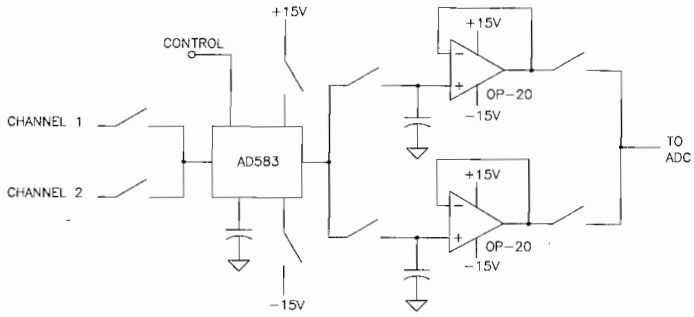



Fig. 5. Sample-and-hold circuit.

that the sample from the first channel is stored on the hold capacitor of the slave sample-and-hold and the start of the first conversion, must be included in the system timing. Also, since the second slave sample-and-hold has to hold its sample for a period equaling two ADC conversion times, the hold capacitor on the second slave must be increased to compensate for the droop.

The dual sample-and-hold configuration was tested and it was determined that it was operating as expected. It was realized, however, that the AD583 was being turned off with as much as 10 V on the hold capacitor, and that the hold capacitor was discharging through the unpowered device. Since it was uncertain as to the effect this would have on the AD583, the situation was corrected by including a third switch on the input to the sample-and-hold, which was connected to the analog ground. After transferring the two samples to the slave sample-and-holds, the AD583 was placed in the "sample" mode with the input grounded, thus allowing the hold capacitor to discharge before turning the device off.

One problem encountered in using the ADC-HC12B was that the logic levels required by the device were equal to the supply voltage which, in this case, is +15 V. Reducing the +15-V levels out of the device to +5 V was accomplished by using CD4050 CMOS inverters which are capable of handling overvoltage signals on the inputs. To pull the START CONVERSION signal up to +15 V, a spare switch in one of the DG211 packages was used.

## VI. Testing the System

The system was tested using a Hewlett Packard test system consisting of an HP9845B computer, an HP3455A digital voltmeter, an HP3325A function generator, and a 6940B multiprogrammer. The function generator was used to provide a programmable dc input signal to the sample-and-hold. The signal was measured using the digital voltmeter. The digital output from the ADC was read by the computer via an isolated input card in the multiprogrammer. Data acquisition and plotting were performed by the 9845B computer. The first test on the system was to determine the linearity of the ADC. With the sample-and-hold module bypassed, the input signal was applied directly to the ADC and the device characteristic was recorded by the computer. The test showed the ADC to be highly linear with only a slight deviation from the ideal

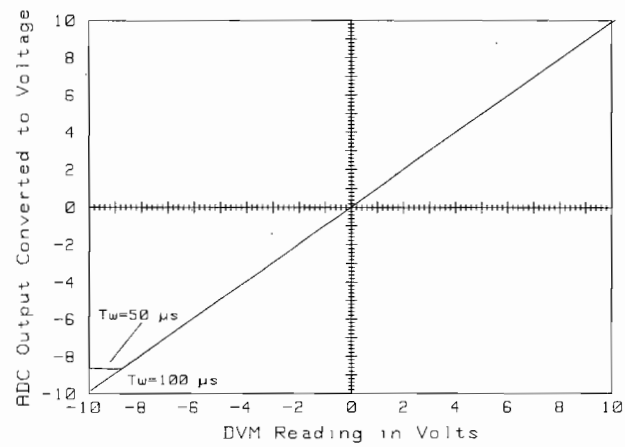



Fig. 6. System response as a function of sample-and-hold warm-up time using a 0.0047-$\mu$F hold capacitor.

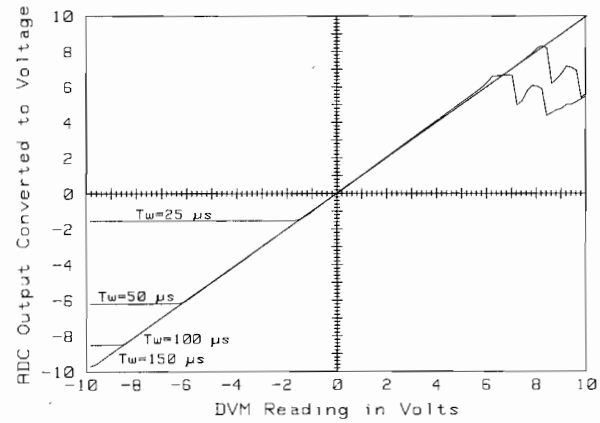



Fig. 7. System response as a function of sample-and-hold warm-up time using a 0.033-$\mu$F hold capacitor.

slope. The second test performed was to compare the warm-up time for the AD583 measured using the oscilloscope and the results obtained using the ADC on the sample-and-hold output. Fig. 6 shows the outcome of the tests performed using a 0.0047-$\mu$F hold capacitor. The data obtained using a 0.033-$\mu$F hold capacitor are shown in Fig. 7. The results obtained using this method agree quite well with those obtained earlier. The warm-up time for the 0.0047-$\mu$F capacitor is shown to be between 50 and 100 $\mu$s, while the value measured earlier was 90 $\mu$s. The warm-up time required for the 0.033-$\mu$F capacitor is shown to be between 150 and 200 $\mu$s. The value measured earlier was 180 $\mu$s. It can also be seen from these graphs that the linearity of the overall system is not affected by the inclusion of the sample-and-hold module, if the correct warm-up time is used.

## VII. Power Consumption

Once it was known that the system was functioning properly, the last area to be examined was the power consumption. The breakdown for the analog portion at room temperature is as follows:

| Device | Power Dissipation |
|---|---|
| ADC-HC128MM | 30 mW |
| AD583 | 6.5 mW |
| OP-20 (×2) | 5.5 mW |
| DG 211 (×3) | 60 mW |
| TOTAL | 102 mW |

The figures above use maximum continuous power dissipation. The value obtained for the AD583 uses the maximum continuous power dissipation multiplied by 176 $\mu$s/4098 $\mu$s, the ratio of ON time to switching period. The total power dissipation of the sample-and-hold module comes to 75 mW, a reduction of 66 percent over that of operating the components continuously. This could be reduced even further by using the DG211 switches only for power switching, where overvoltage protection is required, and on the inputs to the slave sample-and-holds, where low-charge transfer is required. Replacing the other two packages of DG211 switches with DG308 switches would reduce the power dissipation of the sample-and-hold module by an additional 39 mW, to a total of 33 mW. This would make the total dissipation of the analog portion 63 mW. The digital portion of the system consumes slightly more than 25 mW. This is broken down into two areas, the discrete logic and the EPROM. The discrete logic, being all CMOS, consumes only 350 $\mu$W of power. The EPROM, however, consumes 25 mW, contributing greatly to the overall system dissipation, which would total 88 mW if the DG308 switches are used.

## VIII. Conclusions

In some circumstances, the total power dissipation of a mixed digital and linear system can be reduced by operating the linear devices in a low duty-cycle mode. CMOS analog switches provide an efficient way of controlling the power to the switched analog devices.

## References

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