PATARA II: A 64-Channel Solid-State Neutron Detector Readout System with Integrated Analog and Digital Processing for the SNS

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Abstract—The High Efficiency Neutron Detector Array (HENDA) project at the Spallation Neutron Source (SNS), Oak Ridge Tennessee, has driven the need for state of the art radiation detector readout electronics. Readout electronics of this class must support multi-channel inputs while providing a high level of integration and precision. The Patara II ASIC targets this need by integrating a charge sensitive front end followed by analog and digital signal processing that supports the connectivity of 64 detectors. A monolithic biasing system and digital programmability was integrated in order to reduce the amount of required external components on the end system motherboard.

I. INTRODUCTION

THE Spallation Neutron Source (SNS) located at Tennessee's Oak Ridge National Laboratory (ORNL) is the world's most intense pulsed accelerator-based neutron source [5]. This unique neutron source enables world-class neutron scattering research, with an accompanying need for advanced neutron imaging systems including many supporting data acquisition instruments that utilize position sensitive neutron detectors [3]. In particular, the SNS will require a data acquisition system capable of operating a detector array with high spatial resolutions (pixel widths) of 100 μm to 500 μm with a response time of less than 10 μs. A system with these specifications is not currently commercially available [3].

The High Efficiency Neutron Detector Array (HENDA) project was initiated to meet the unique imaging needs of the

SNS. A deliverable of this project is a highly integrated, mixed-signal detector readout system. The solid-state detector is fabricated utilizing modern design and micro-fabrication techniques to provide high channel counts on a single microchip. When mated with custom readout electronics implemented as an application specific integrated circuit (ASIC), this approach can yield a highly integrated, high channel count neutron detector system

To address the need for highly integrated readout electronics, a custom readout ASIC (Patara I) was specifically designed to interface to a novel thin film neutron detector [3]. This ASIC integrated 16 analog processing channels, each consisting of a charge sensitive preamplifier [3] and a gated baseline restore semi-Gaussian shaper [3]. The predecessor Patara II ASIC detailed in this paper, utilizes the Patara I front end and further incorporates the mixed signal circuitry necessary to interface the SNS system in the digital domain. A single Patara II ASIC can interface to 64 neutron sensors while providing the channel DC biasing and encoded channel event.

This paper is organized into five sections. *Section II* provides a system overview of the Patara II ASIC with a summary of the system level requirements. In *Section III* a design overview of the major circuit blocks is given. In *Section IV* the ASIC testing methodology is discussed and measurement results from the Patara II ASIC are provided. Finally, conclusions from this research and a discussion of future work are presented in *Section V*.

II. PATARA SYSTEM OVERVIEW

A. Neutron Detector [3]

The Neutron sensor developed for the HENDA project is a novel thin-film coated, silicon diode detector. This detector utilizes evenly spaced etched cavities on its surface as shown in Fig. 1. a technique that provides increased detection efficiency versus non-etched surfaces.

When a neutron event occurs by colliding with the surface of the detector, an ionic reaction will occur releasing an alpha particle. When this event occurs over a semiconductor, in this case silicon, the alpha particle collides with the silicon lattice creating a charge proportional to the energy required to create

The surface and the holes are filled with neutron reactive material such as B-10 or Li-6F.
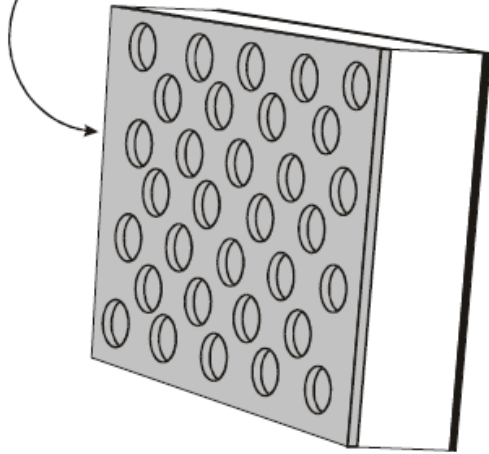

Fig. 1. Thin film neutron detector with evenly spaced etched cavities.

an electron-hole pair. This charge can then be converted to a voltage potential and discriminated versus the lower level discriminator (LLD) setting.

Background gamma radiation will also create charge within the detector substrate when a neutron event occurs. This excess charge will also contribute to the input charge presented at the front end of the analog readout electronics. Simply reducing the LLD voltage potential can increase the detection efficiency; however the risk of including these background radiation events increases as the LLD is lowered [6]. From [6] the optimal LLD setting was found to be 300keV.

A. Analog Front End [3]

The detector has a final expected capacitance of 5 pF to 10 pF, and an expected leakage current of 5 nA. The charge sensitive preamplifier (CSPA) must be DC coupled with the detector and must meet the following specifications:

1. Low input referred noise: ≤ 1500 RMS electrons for a detector capacitance of 5 pF,
2. Positive or Negative charge input,
3. Detector leakage current compensation,
4. Active pole/zero compensation network,
5. Preamplifier gain adjustment.

A pole-zero cancellation technique must be implemented in order to optimize the response of the CSPA and to avoid charge pile-up. One real pole must be introduced after the pole-zero cancelation. This can be implemented by introducing a voltage-amplifier based real pole.

Following the first real pole of the system, a unipolar four-pole complex-conjugate semi-Gaussian shaper is introduced. This stage also introduces a baseline restorer to set the DC level of the analog processing chain. A unipolar response is desired versus the bipolar counterpart due to a superior signal-to-noise ratio (SNR), and due to the ability of maximizing the dynamic range of the shaper. The semi-Gaussian response is a compromise between maximum theoretical noise performance and return-to-baseline time (pulse rate) capability. Along with the first real-pole from the CSPA, four poles can adequately approximate a semi-Gaussian response [7]. Fig. 2 illustrates the analog processing channel block diagram fabricated in the Patara I ASIC.

B. Patara II Detector Readout Channel

The analog processing channel presents a semi-Gaussian voltage pulse above a DC voltage baseline that will have an amplitude dictated by the charge gain of the CSPA and the total input charge. The radiation event detection can be amplitude detected or level detected. Amplitude digitization, in this application, is unnecessary since a single radiation event is being processed. Therefore, level detection is implemented via a single comparator.

The addition of the event discrimination comparator (shortened to discriminator) raises the need to determine the DC operating range and overdrive requirements. As shown in [6], the optimal discriminator level is 300keV. In silicon the energy required to create an electron-hole pair is 3.6eV. The number of electron-hole pairs corresponding to 300keV can be found by

$$\frac{300\ keV}{3.6\ eV} = 83,333\ electron-hole\ pairs. \tag{1}$$

The unit charge of an electron is known to be 1.6 x 10^{-19} C. This translates to

$$83,333 \times 1.6 \times 10^{-19} = 13\ fC. \tag{2}$$

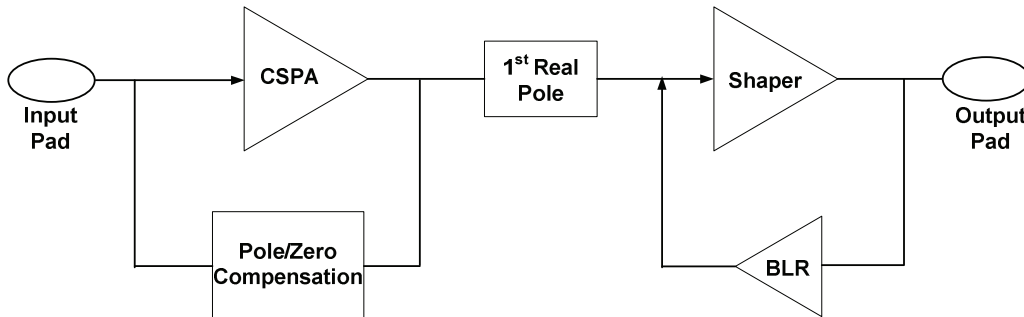The charge gain from the input of the CSPA to the output of the shaper is nominally

Fig. 2. Analog processing channel block diagram implemented on the Patara I ASIC.

$$9.6\,\frac{mV}{fC}. \tag{3}$$

Therefore, the output of the shaper associated with 300keV in silicon is approximated by multiplying eq. (2) and eq. (3):

$$9.6\,\frac{mV}{fC}\times13\ fC=125\,mV. \tag{4}$$

This is the voltage potential above the baseline restorer (BLR) potential. Nominally the BLR level will be 150mV. This voltage level was chosen to ensure that the devices that comprise the shaper stay in the saturation mode of operation. The resulting discrimination level with respect to ground is

$$BLR\ Level+LLD\ Level=150\,mV+125\,mV=275\,mV. \tag{5}$$

From here it is obvious that the discriminator must be ground sensing. The other requirement is that the discriminator has a large gain in order to operate under low overdrive conditions. An illustration of the processing channel with the discriminator is shown in Fig. 3 below.

To meet the gain requirements a cascaded comparator configuration was used. This topology isolates the second discriminator level from the actual LLD setting and allows for the second stage to operate at a larger overdrive condition. Digitally buffering the second comparator output will also increase the signal integrity.

The next requirement is to digitally process the neutron event and synchronize it with the SNS backend. Each channel must therefore incorporate input registering and edge detection circuitry. The edge detection circuitry allows for direct synchronization with an external clock. However, an on-chip clock may introduce a significant amount of input referred noise. Therefore, an asynchronous system must also be implemented as a secondary resource. The single channel block diagram implemented on the Patara II ASIC is illustrated in Fig. 4

C. Patara II System Level Description [8]

The core of the Patara II ASIC is composed of 64 of the detector readout channels discussed in the last section. The output of each channel is a digitally registered channel state.
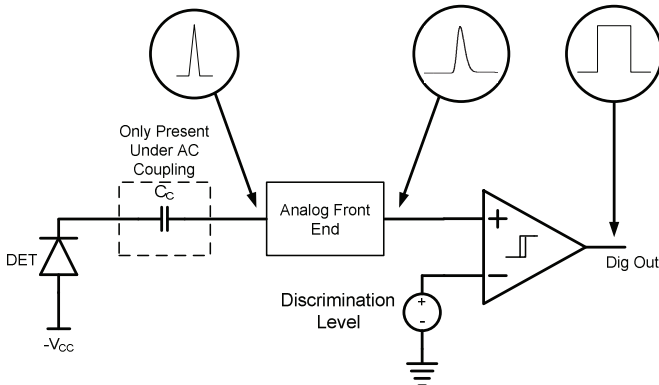

Fig. 3. Signal processing channel with discriminator and waveforms.

If an event occurs on a given channel, the associated digital output will be a logic 1. Due to the parallel nature of the signal processing core, priority must be given to a channel in the case where multiple events occur. To accommodate multiple events, a 64-bit parallel priority encoder was incorporated to process the digital outputs of the 64-channel core. Channel 0 has the highest priority while the rest of the channels are given priority sequentially from channel 0.

Parallel processing of the priority encoding was implemented to guarantee minimal propagation delays. The digital circuitry must be fast enough to ensure that the backend processing between the SNS system and the ASIC has completed by the next radiation event. With a clock rate of 10 MHz, the maximum processing rate will be 5 MHz after handshaking between the ASIC and the SNS host. This allows the digital processing in the ASIC to be complete within approximately 200ns of an event.

Binary encoding of the prioritized channel event will reduce the data bus width between the ASIC and the SNS system. This can be implemented with standard combinational logic and a 6-bit output. The binary encoding is 0-based and will therefore present the need for a valid-data flag to the host. When the valid-data flag is a logic 1, the SNS system will read the state of the 6-bit channel word and then send back a master reset to all registers. Ensuring that all registers in the ASIC are held indefinitely until the SNS host applies a reset will eliminate any system chattering due to concurrent radiation events. This protocol dictates an 8-bit bus between the ASIC and the SNS host consisting of a 6-bit binary encoded channel event word, a 1-bit valid data flag, and a 1-bit master reset.

To increase drive capability and noise immunity, Low Voltage Differential Signaling (LVDS) is implemented on the 8-bit bus. The drivers and receivers are integrated into the ASIC.

The baseline restorer level and the discriminator level are not fixed inputs and will need to be adjusted by the SNS host in order to achieve optimal operation. To accommodate this need, an 8-bit current driven digital-to-analog converter with an adjustable offset is designed. The BLR level and the discriminator level will have a dedicated DAC to internally bias the circuitry. A bandgap voltage reference (BGR) cell is also required to set the biasing for the DACs.

An internal test mode circuit is integrated to generate charge and stimulate an individual channel input. The test mode circuit connects a capacitor to the input of the channel under test and pulses a bias voltage across the capacitor to generate a
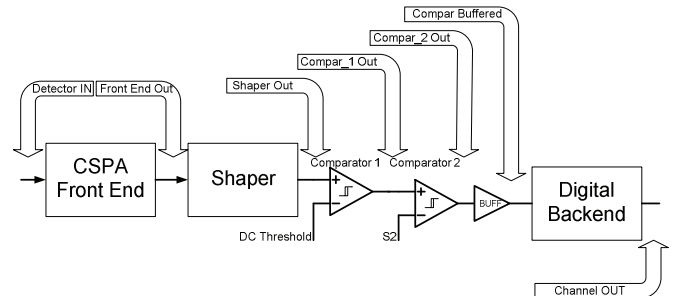

Fig. 4. Signal processing channel with discriminator and waveforms.

charge equal to the capacitance multiplied by the bias voltage. A dedicated 8-bit DAC is used for this voltage bias in order to adjust the applied input charge.

A serial interface is implemented so that the SNS host can set the digitally adjustable peripherals. This includes the BLR DAC, discriminator DAC, test mode DAC, the CSPA feedback resistance, and the channel test mode. The serial interface is daisy-chain compatible so that any number of Patara II ASICs can be used on a single motherboard. A block diagram of the Patara II ASIC is illustrated below in Fig. 5.

III. MAJOR CIRCUITRY DESIGN

A. Charge Sensitive Preamplifier [2]

The CSPA employs a novel pole-zero cancellation circuit based on the single MOSFET feedback network proposed in [9]. This approach reduces silicon area with the use of active devices while enhancing the pole-zero cancellation scheme by improving tracking over the dynamic signal range.

A unique feature of this amplifier is the ability to adjust for leakage current polarity. This allows for the anode or the cathode of the detector to be connected to the input. The amplifier gain can also be adjusted to account for differing neutron reactive material.

To reduce noise contributions, the input device is sized such that the gate-source capacitance, C_{gs}, is 1/3 of the detector capacitance. The final input FET size is W/L = 1250 μm /0.4 μm. The CSPA circuit concept is shown in Fig. 6. Lower level design details can be found in [4] and [2].

B. Semi-Gaussian Shaper [1]

The shaper consists of a voltage-to-current (V-to-I) converter operational transconductance amplifier (OTA), followed by two pairs of complex-conjugate poles. It also has an active baseline restoration circuit, consisting of an OTA and hold capacitor, where C = 5 pF.

The circuit topology chosen to implement the four complex conjugate poles was an *R-Lens filter*[11]. This filter topology has the benefit of passing low frequencies relative to g_m-C filters, high linearity, voltage or current input, and a straight
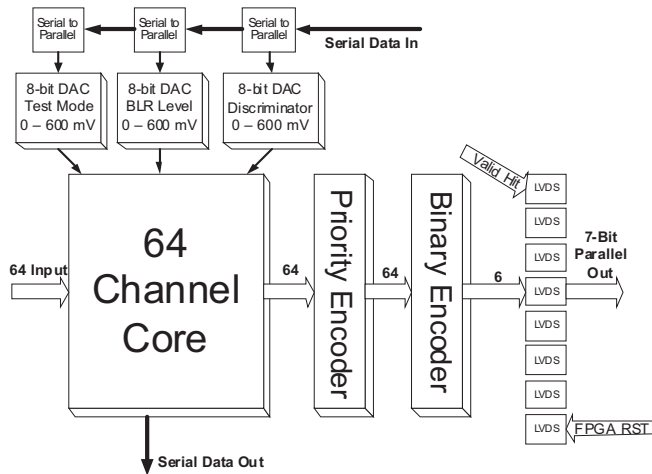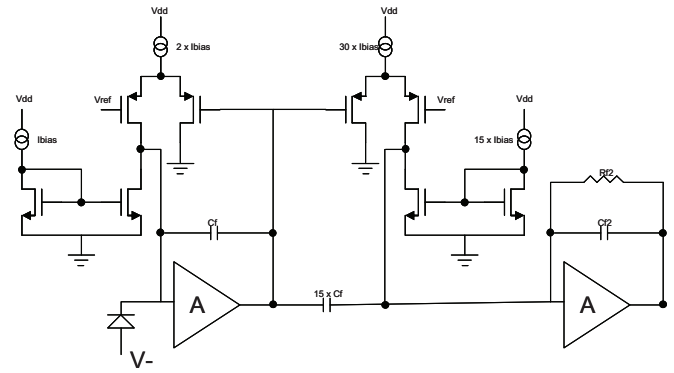

Fig. 6. CSPA concept with a novel resistive feedback element

forward implementation with an even number of poles. The semi-Gaussian shaper concept is shown in Fig. 7 below. Design details can be found in [4] and [1].

C. Ground sensing Discriminator [8]

PMOS input devices were used in the design of the comparator to enhance ground sensing capability. In many cases a PMOS differential pair can sufficiently make up the input stage to the comparator. In this design, PMOS source-followers (devices M_8 and M_{14} in Fig. 8) were used to buffer the input to an NMOS differential pair (M_1 and M_2). This allowed for a below-ground sensing capability since the drains of the input buffers are common to ground, whereas a differential pair normally has active loading connected to the drains of the input devices.

The drawback to this topology is the open loop gain. The gain of the differential pair is small due to the diode connected loads. Therefore the gain of the comparator is dominated by only the common-source second stage. For this reason a cascaded comparator configuration was implemented.
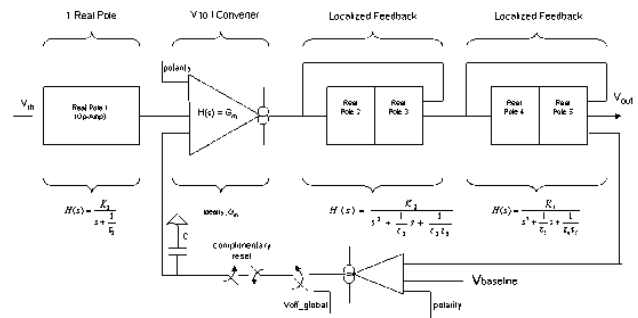

Fig. 5. Patara II ASIC block diagram.

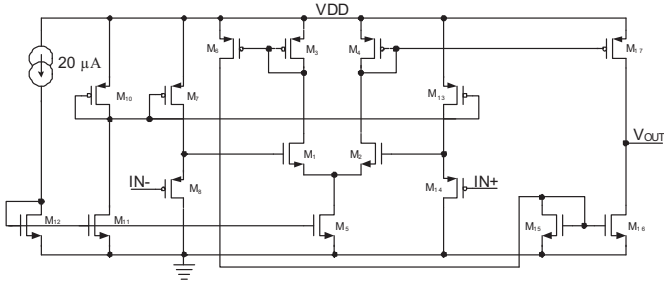Fig. 7. Semi-Gaussian shaper concept.

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Fig. 8. Comparator topology used in the cascaded discriminator

D. 8-bit Current Driven DAC [8]

The DAC was designed to have a dynamic range of 600mV. This resulted in a 1 LSB resolution of

$$1\,LSB = \frac{600mV}{2^N} = \frac{600mV}{256} = 2.34\,mV. \tag{6}$$

The 1 LSB current, I_{LSB}, was chosen to be 1 µA. This translates to a transimpedance ratio (current-to-voltage conversion) of

$$\frac{V_{out}}{I_{in}} = \frac{2.34\times10^{-3}}{1\times10^{-6}} = 2.34\times10^{3}\,\Omega \tag{7}$$

The DAC architecture is based on the topology shown in Fig. 9 [10]. Binary weighted current sources are digitally switched and summed at the current summing node of the op amp. The transfer function of the DAC is

$$V_{out} = V_{off} - R_F \cdot I_{LSB}(m+q) \tag{8}$$
$$where, \quad 0 \le m \le (2^N - 1).$$

The term q is the scaling factor for the offset current with respect to I_{LSB}, and N is the resolution of the DAC in bits. The offset current is used to provide the ability to change the output offset of the DAC with a fixed V_{off} potential.

The LSB current is generated from the integrated BGR. The reference current from the BGR was designed to be 16 times (half the bit range or 2^4) the LSB current to provide better current matching throughout the binary weighted current mirrors. The LSB current is found to be
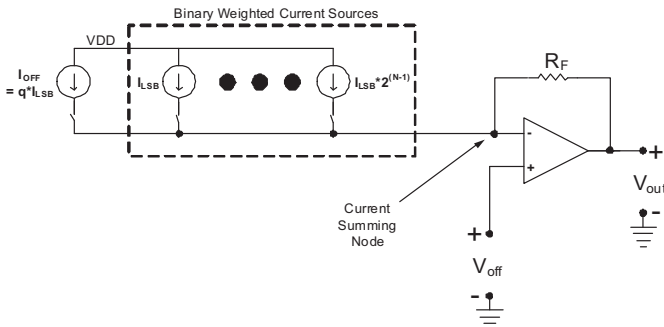
$$I_{LSB} = \frac{V_{bgr}}{16 \cdot R_{bias}}. \tag{9}$$

Plugging equation 9 into 8 yields

$$V_{out} = V_{off} - V_{bgr} \cdot \frac{(m+q)}{16} \cdot \left(\frac{R_F}{R_{bias}}\right). \tag{10}$$

The ratiometric relationship between R_F and R_{bias} compensates for any absolute resistance value changes introduced during fabrication. If careful monolithic construction is engineered, the resistor values will track to ±2%.

Two important parameters can be extrapolated from equation 10. The slope of the DAC can be written as

$$slope = -\frac{V_{bgr} \cdot R_F}{16 \cdot R_{bias}} \tag{11}$$

and the y-intercept as

$$y - int. = V_{off} - q\left(\frac{V_{bgr} \cdot R_F}{16 \cdot R_{bias}}\right) \tag{12}$$

Any change in V_{bgr} across process will directly affect the slope and the offset current in the y-intercept. If the offset current is disabled, the offset voltage will set the y-intercept.

E. Readout Channel Digital Backend

The use of bistable multivibrator circuits allow for simplified synchronization with a system clock. This design specifically utilizes D-Flip-Flops as the building blocks. To detect an edge, the sequence of events must be a logic '0' on the first clock, and a logic '1' on the second clock. Therefore only two D-Flip-Flops and one AND gate are necessary for the edge detection circuitry.

An input register is required to handle the potential short walk time from the comparator. Having the comparator drive the clock terminal of the register will ensure the comparator transition is captured and held until a master reset is applied. The synchronous digital backend is shown in Fig. 10. To implement the asynchronous system the input registered is directly passed to the output register. Two-port multiplexers
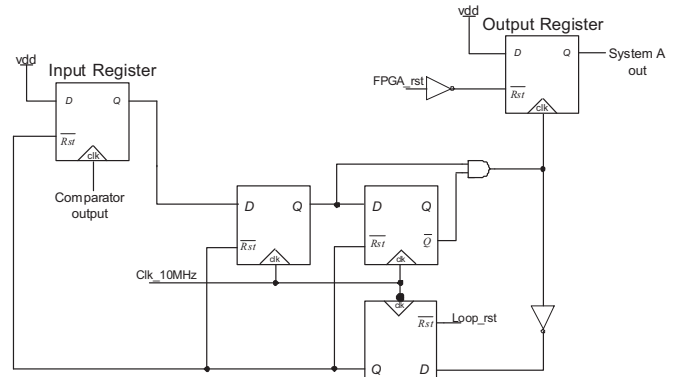

Fig. 9. Current driven DAC architecture [10]

Fig. 10. Synchronous digital backend

are used to switch the signaling between the two systems.

F. Patara II ASIC Micrograph

The physical design of this ASIC was fabricated in the Taiwan Semiconductor Manufacturing Company's (TSMC) 0.35-µm bulk CMOS process available through a MOSIS shared project run. The overall physical dimensions of the die are 6.5 mm by 6.7 mm. The final ASIC micrograph is illustrated in Fig. 11 below.

IV. MEASUREMENT RESULTS

The test bench for the ASIC utilized an external FPGA and digital I/O modules that interface via custom-developed LabVIEW software. A custom motherboard set the external biasing and cabling between the ASIC and the FPGA. Spy points were hooked to the upper and lower channels to observe the analog circuitry waveforms across the chip. A chip-on-board packaging scheme was implemented to interface the 226 bond pads.

The internal test mode was utilized for channel verification. However, variation in the monolithic capacitor will contribute to some amount of the variation in the observed waveforms across the chip.

A. CSPA Measurement Results

The CSPA illustrated similar results as shown in the Patara I ASIC. A comparison of a 13fC event observed on channel 0 and 63 is illustrated in Fig. 12.

B. Semi-Gaussian Shaper

A revision to the baseline restorer OTA was introduced in the Patara II ASIC to reduce the offset observed in the testing results from the Patara ASIC. The output waveform with a
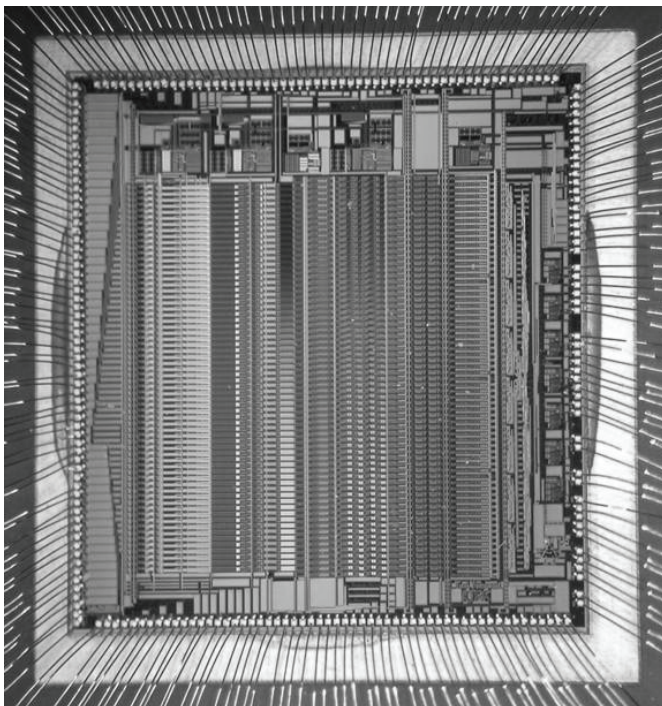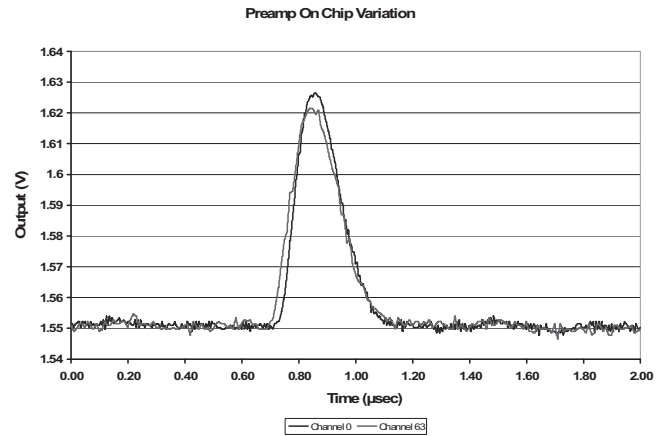
Fig. 12. Measured preamplifier variation across chip

13fC input across chip is shown in Fig. 13 and the offset measured chip-to-chip is illustrated in Fig. 14.

C. LLD Setting vs. System Accuracy

An important parameter to understand is the LLD setting versus a fixed input charge. If the LLD setting is within the noise of the baseline a constant reading from channel 0 will occur. This is due to the priority encoded processing.
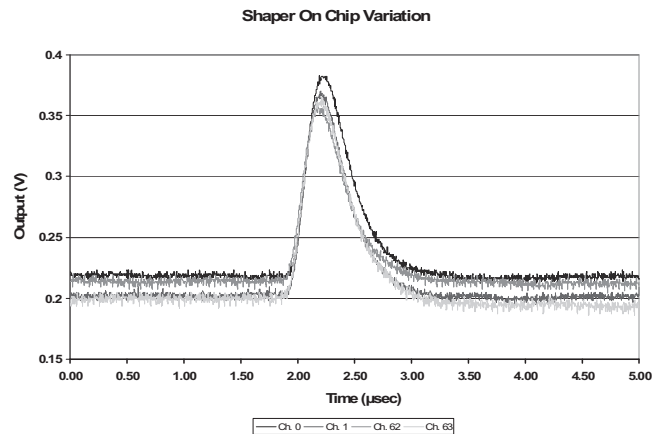
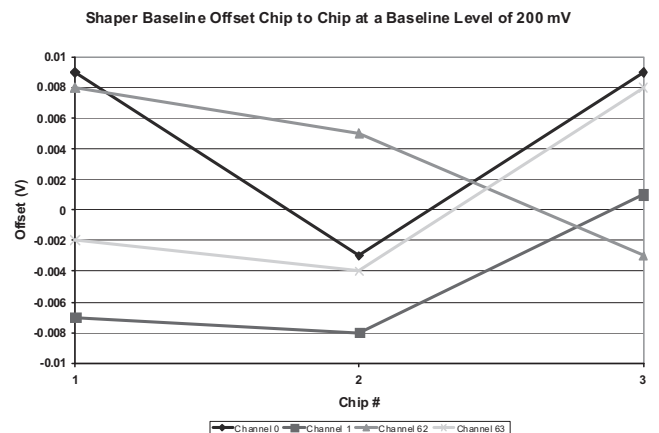Fig. 13. – Measured shaper variation across chip

Fig. 14. Measured shaper baseline offset variation at a baseline of 200-mV

Fig. 11. Patara II ASIC micrograph.

Therefore studying channel 1 onwards is necessary. By sweeping the discriminator level and applying a fixed amount of events on the channel under test at each discriminator level will capture the LLD setting versus accuracy—where accuracy is defined by the amount of detections divided by the total applied events.

Fig. 15 illustrates this test at a BLR level of 220mV and an input charge of 13 fC. It is apparent that the system is 100% accurate across all channels at an LLD setting of 0.35V to 0.37V.
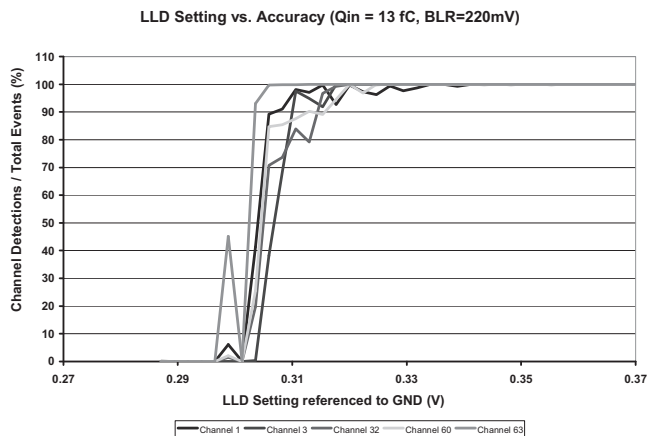

Fig. 15. Measured percent accuracy across multiple channels

D. Noise Results

For ^{10}B our expected dynamic range was 300keV – 1.47MeV (~83k – 410k e-h pairs). A desired threshold uncertainty of approximately 1/10 of the lower end is 30KeV. Assuming a 6σ noise distribution for this requires rms noise to be less than approximately 1300e. This means the noise, as shown in Fig. 16, is within specification for 2pF –6pF detector capacitance which is acceptable for this system. The exhibited noise for this is higher than for the original Patara I [4] with the observed noise on the test board being the primary suspect for the increase.
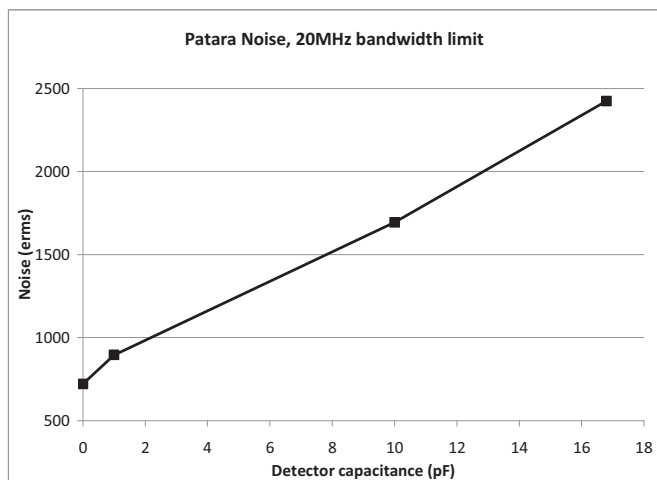

Fig. 16. Patara II input referred noise

V. CONCLUSION

A 64-channel ASIC for the HENDA detector has been developed. The ASIC is designed specifically for implementation at the Spallation Neutron Source and implements the functionality needed to read out the HENDA thermal neutron detector array. The ASIC is comprised of 64 channels of charge readout and implements a priority-encoded digital output to the SNS back-end readout boards.

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