If the bit number of the DA converter corresponding to the heater bias power in the initial setting were D and the setting error from the final value were d, the control deviation to P_h comes to

$$\Delta P_1 = \frac{2d}{D} P_h. \tag{1}$$

Let the deviation at the kth resetting of the DA converter by computer control be ΔP_k, the next relation is obtained from a consideration of the feedback loop

$$\Delta P_k = \frac{\Delta P_{k-1}}{1+G}, \qquad k = 2, 3, \cdots, n \tag{2}$$

where G is the open loop gain for small signals in the analog feedback system consisting of the temperature detector, preamplifier, adder, and heater.

At nth resetting, ΔP_n can be expressed as

$$\Delta P_n = \frac{2dP_h}{(1+G)^{n-1}D}. \tag{3}$$

Consequently, the control eror ϵ after resetting of n times comes to

$$\epsilon = \frac{2d}{(1+G)^{n-1}D}. \tag{4}$$

The number of resetting times is meaningful until the step of the controlled variable comes less than the power resolution ΔP_r by the DA converter

$$P_h - P_{n-1} < \Delta P_r \tag{5}$$

where $\Delta P_r = 2P_h/D$ and $P_{n-1} = P_h - \Delta P_{n-1} \cdot P_{n-1}$ is the measured heater bias power at $(n-1)$th times.

From (3) and (5), the following expression is obtained:

$$n > 2 + \frac{\log d}{\log (1+G)}. \tag{6}$$

In actuality, increasing n over a certain limit may not improve the error limitlessly. The upper limit of n can be determined as the minimum integer which satisfies the inequality (6).

For example, the data of $d = 10$ and $G = 10$ have been obtained at 10-mW power level, for the example described later. In this case, n comes to 3. The resolution $1/D$ of the DA converter is $1/500$. As a consequence, the control error becomes 3.3×10^{-4} from (4) by substituting these data.

Experimental Results

The temperature control system has been applied to a laser power calorimetric measurement method. The calorimeter uses a thermopile unit as a thermal load which is similar to the one described in [2]. The temperature detector and cooler consist of module type Peltier element made of Bi-Te alloy. The preamplifier for temperature detecting has a gain of 10^5.

This laser power measuring experiment has been performed at the 10-mW level using a He-Ne laser. In order to shorten measuring time, the heater bias power for initial setting has been preliminarily determined by performing the previously explained isothermal control procedure. In actual power measurement, control of the DA converter begins with the voltage corresponding to the predetermined heater bias power.

The output voltage of the temperature detector in the control process has been obtained through the preamplifier as shown in Fig. 2. In this experiment, three resettings were used based on the calculations in the earlier section. Laser power was measured five times in order to compensate for temperature drift. The maximum difference of the output voltage for laser power on and off has been estimated as 0.075 μV from Fig. 2. It corresponds to 4×10^{-5}°C in temperature from the responsivity 1.8 mV/°C. In power, it comes to 3.6 μW from the responsivity 21 μV/mW. Then, the control error

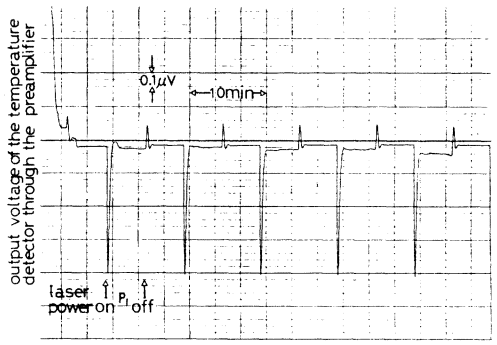

Fig. 2. Control deviation in the calorimetric measurement.

is estimated as 3.6×10^{-4} at a 10-mW power level. It is comparable to the expected error from analysis.

Conclusion

An advanced temperature control for calorimetric power measurement has been described. An analysis shows that even if the initial setting were rough and the loop gain of the control small, the method is effective in reducing error due to temperature control by resetting the DA converter a few times. The experimental result correlates well with the analysis. The method has the advantage of achieving precise temperature control without adjusting the parameters of the feedback system.

Acknowledgment

The authors wish to thank I. Yokoshima, Chief of the Radioelectronics section, and the members of that section for their helpful discussions and critique of this manuscript.

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Low-Power Operation of the SBP9989 16-Bit I²L Processor

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***Abstract*—Tests of maximum usable clock frequency as a function of injection current have been made on six Texas Instruments SBP9989 processors. In addition, the output characteristics for the logic output low condition have also been measured for the HOLDA terminal. All of these measurements were made over the full military temperature range. These tests have shown that the SBP9989, a 16-bit I²L processor with internal signed multiply and divide instructions, will operate at relatively high clock frequencies at low-power levels and consequently is well suited to high-performance low-power instrumentation and digital filtering applications.**

Manuscript received January 17, 1983. This work was supported by the Physical Security Systems Directorate, Electronic System Division of the Air Force Systems Command, Hanscom Air Force Base, MA 01731.

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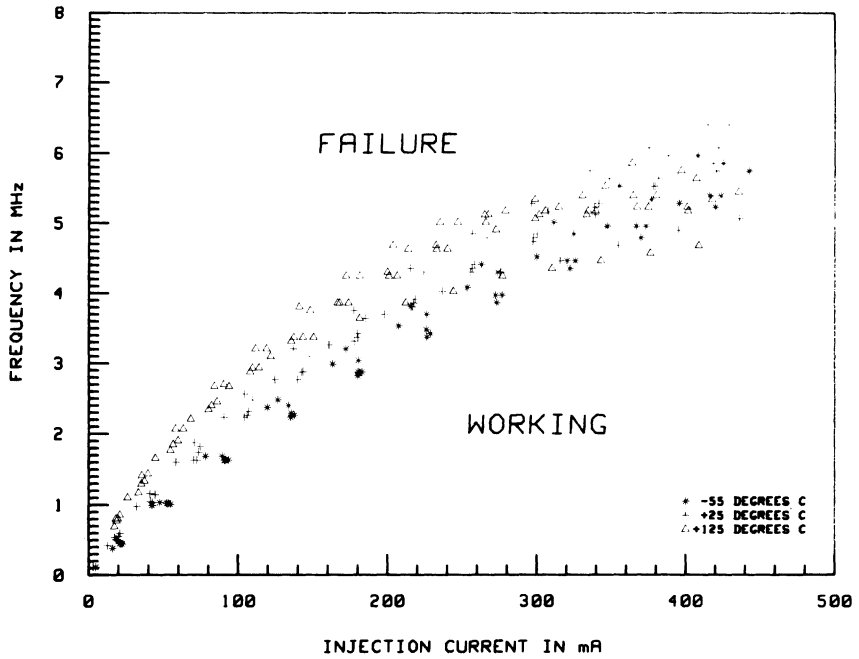

Fig. 1. Maximum usable clock frequencies as a function of injection current for the SBP9989 I^2L microprocessor.

Introduction

The designer of high-performance low-power instrumentation or digital filtering systems has a continuing requirement for low-power processors with on-chip 16-bit signed multiply and divide instructions. Our tests have shown that the Texas Instruments SBP9989, a 16-bit I^2L (current injection logic) processor with internal signed multiply and divide instructions, will operate with low injection currents at relatively high clock rates.

In the two earliest papers on what is now known as I^2L, the authors noted that for each I^2L stage the propagation delay was inversely related to the power dissipation [1], [2]. As a result of this relationship the maximum usable clock frequency for an I^2L chip might be expected to be a direct function of the square of the injected supply current; however, this does not appear to be the case for the SBP9989. Because the relationship between the maximum operating frequency and the injection current is an important design parameter, the maximum usable clock frequencies as a function of injection current have been measured for six samples of the SBP9989. These tests were made over the injection current range of 0 to 420 mA at −55°C, room temperature, and +125°C, and the results of the tests are shown as a scatter plot in Fig. 1.

Test Procedure to Measure Maximum Usable Clock Frequencies

A schematic diagram of the test connections is shown in Fig. 2. The test procedure consisted of first setting the injection current to the desired test value and then forcing the processor under test to execute a continuous series of NOP instructions. The actual NOP instruction used was JMP which has the binary OPCODE (00010000) and which results in the processor fetching the next instruction which is always JMP. When the processor was operating in a satisfactory manner, the output of address line A14 was equal to $f_c/12$, the processor clock frequency divided by 12; failure was assumed to occur when the output on A14 differed from $f_c/12$ by an arbitrary amount, usually set at 1 percent.

Test Procedures to Measure HOLDA Terminal Characteristics

To calculate optimum values for pull-up resistors, the designer of a low-power system using the SBP9989 would need characteristic curves for output terminal sink currents as a function of the output

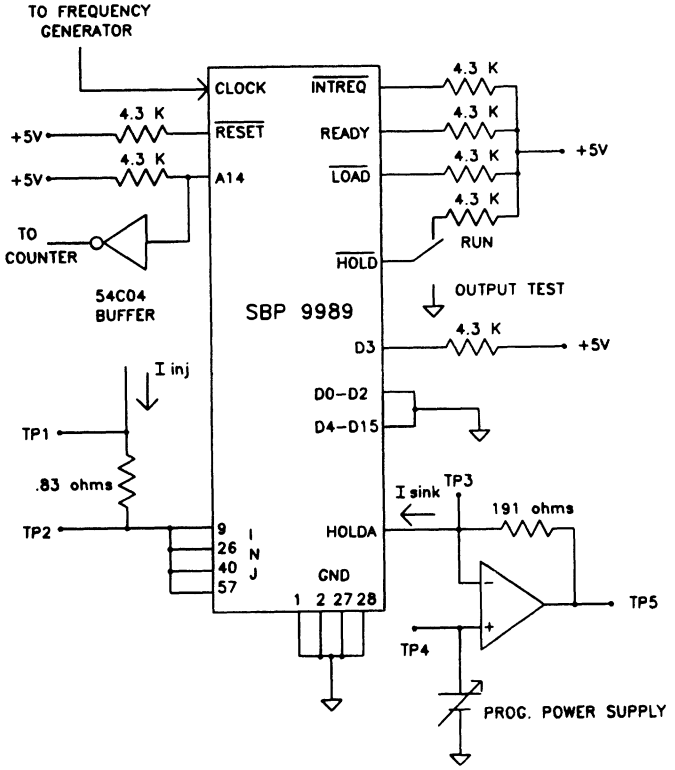

Fig. 2. Schematic diagram of test circuit.

terminal voltages. These characteristics were measured on the HOLDA terminal and are representative of all output terminals, they are shown in Figs. 3 and 4. A simplified version of the test circuit used is shown in Fig. 2. Here, the test procedure was to first set the temperature of the environmental chamber, then set the injection current; next, the programmable power supply voltage was stepped from zero to whatever maximum resulted in a terminal current of 16 mA. The voltage applied to HOLDA was checked by measuring from TP3 to ground, the current at each voltage increment was calculated by measuring the voltage between TP5 and TP3 across the 191-Ω resistor. The measurements were made on an HPIB–IEEE 488 system using all Hewlett-Packard system components.

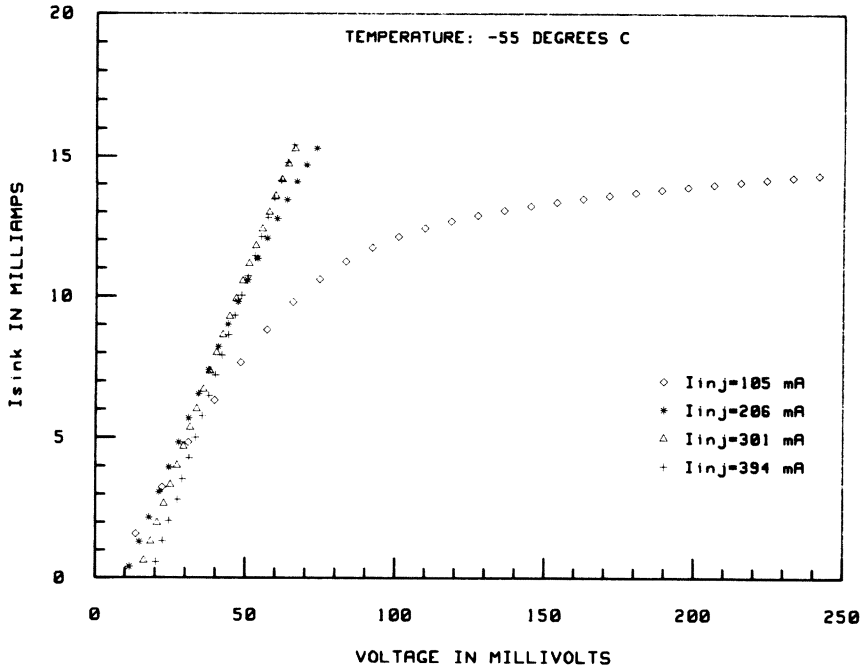

Fig. 3. HOLDA terminal characteristics for SBP9989—sink current as a function of voltage with temperature at −55°C.

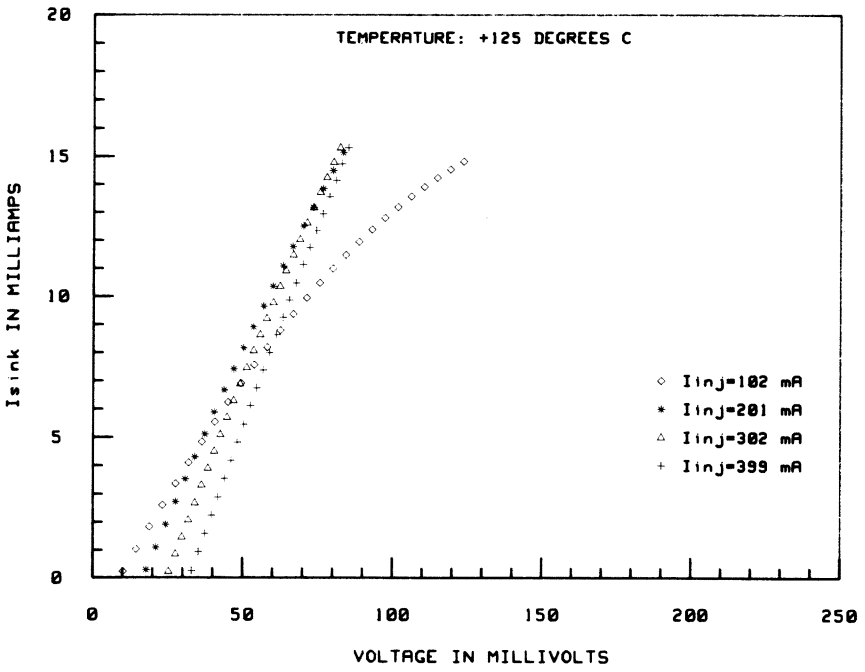

Fig. 4. HOLDA terminal characteristics for SBP9989—sink current as a function of voltage with temperature at +125°C.

Discussion of Test Results

According to Texas Instruments the SBP9989 is guaranteed to operate at a clock frequency of 4.4 MHz at a nominal injection current of 400 mA over the temperature range −55°C to +125°C; our tests (as demonstrated in Fig. 1) have supported these claims and provided a considerable amount of new information which is not available from the manufacturer but is of great importance to the designer of low-power systems. It is of particular interest to note that one of the devices was still operating on an injection current of 4.9 mA at a clock frequency of 0.11 MHz.

Figs. 3 and 4 are, in reality, the collector characteristics of the output transistor driving the HOLDA terminal. These curves show I_{sink}, the HOLDA terminal current with HOLDA logically low, as a function of the HOLDA terminal voltage. Although these characteristics were measured for all six devices, the curves shown are typical. In making these tests, the HOLDA terminal current I_{sink} was limited to a maximum of 16 mA. We note that the curves show a voltage offset with zero current. Presumably this effect is caused by the internal resistance of the injection current paths within the silicon chip since the amount of the offset is related to the injection current.

To demonstrate an application of these test results, we note from Fig. 1 that at an injection current of 120 mA all of the devices tested would operate at a clock frequency greater than 2 MHz over the temperature range −55°C to +125°C. According to the SBP9989 data book, the potential between the injection terminals and ground for a 120-mA injection current is approximately 0.8 V, this results in an estimated power dissipation of 96 mW. At a clock frequency of 2 MHz and a cycle time of 0.5 μs, the total time required for a

signed multiply instruction would be equal to 56 clock cycles multiplied by 0.5 or 28 μs. These two results for power dissipation and 16-bit signed multiplication time compare favorably with those obtained with 8-bit CMOS processors using external multipliers.

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A Simple Stray-Free Capacitance Meter by Using an Operational Amplifier

SEIJI KURODA

***Abstract*—A simple operational amplifier circuit known as a charge amplifier has an advantage of measuring capacitance independent of stray capacitance. Capacitance down to 0.03 pF could be experimentally measured with ease and the theoretical limit of measurement is discussed. Also the direct measurement of the electrostatic induction coefficients of a system of conductors by the circuit is introduced.**

I. Introduction

In measuring a small capacitance, especially less than 1 pF, cancellation of stray capacitance, which is usually introduced by the connection wires and the environment, is essential. The transformer bridge has been used for the precise measurement of a small capacitance because it can compare the capacitances of two capacitors independent of the strays. However, the construction of such a transformer bridge is not an easy task. Our capacitance meter, on the other hand, is simple and can measure capacitance independent of stray capacitance as well, though may not be suited for the most precise measurement of capacitance.

II. Circuit Description

Fig. 1 shows the scheme of our capacitance measurement with an op-amp circuit. C_x is a capacitor of unknown capacitance and the strays around C_x can be represented by C_{s1} and C_{s2} in most cases. C_s is a standard capacitor and R_f is inserted to maintain the stability of the circuit. By setting the frequency f_0 of the input ac voltage V_i to be midway between $1/(2\pi R_f C_s)$ and the cutoff frequency of the op-amp, the output voltage V_o is given by

$$V_o = -\frac{C_x}{C_s} V_i \tag{1}$$

independent of C_{s1} and C_{s2}. Note that C_{s2} is not charged because there exists no potential difference across it. Therefore C_x can be determined by measuring V_o. In some cases, there exists a direct coupling between the connection wires of C_x and the resultant stray capacitance C_{s3} as shown by the dotted line in Fig. 1 must be considered. However, C_{s3} can be eliminated by using shielded cables for the connection of C_x. The use of the shielded cables only increases C_{s1} and C_{s2} and does not affect the measurement of C_x.

For the circuit used in the experiments, f_0 is 1 kHz, CA3140(RCA) is chosen as the op-amp for its low bias current and high input impedance characteristics, a polystyrene capacitor of 296 pF is used as the standard capacitor C_s, and R_f is 300 MΩ. In addition, a band-pass filter of a center frequency f_0 = 1 kHz and a bandwidth Δf = 100 Hz is added to reduce the effect of the noise introduced by the op-amp. The input voltage and the output voltage are recorded by a storage oscilloscope to read V_i and V_o.

Manuscript received July 22, 1983.

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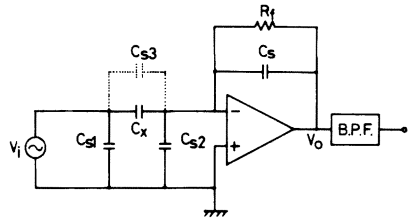

Fig. 1. Circuit diagram of the capacitance meter (op-amp: CA3140(RCA); oscillator: V_i = 15 V, f_0 = 1 kHz, C_s = 296 pF, R_f = 300 MΩ; band-pass filter: f_0 = 1 kHz, Δf = 100 Hz. C_x is the unknown capacitance and C_{s1}, C_{s2}, and C_{s3} are the stray capacitances).

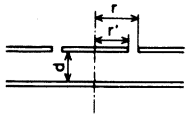

Fig. 2. Capacitor with a guard ring used in the experiments.

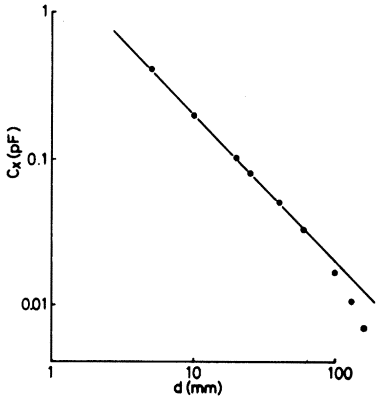

Fig. 3. Results of the capacitance measurement (plots) with the calculation (solid line).

III. Experiments

We made a parallel-plate capacitor with a guard ring as illustrated in Fig. 2 for C_x, whose capacitance is given by

$$C_x = \epsilon_0 \frac{\pi(r' + r)^2}{4d} \tag{2}$$

where ϵ_0 is the permittivity of free space, r' and r are the radius of the capacitor electrode and the guard ring, respectively, and d is the separation of the plates. For r' = 8 mm and r = 9 mm, the calculated capacitance is shown by the solid line as a function of d in Fig. 3. The upper electrode of radius r' is connected to the inverting terminal of the op-amp while the guard ring is to the ground and the lower plate is to the oscillator. The plots in Fig. 3 are the measured capacitance of C_x and agree well with the calculation for d smaller than 60 mm. For d greater than 60 mm, the measured capacitance becomes smaller than the calculation because the electric field lines inside the capacitor leak substantially due to the finite dimension of the guard ring, and therefore the capacitance becomes smaller than that given by (2). Shielded cables of various length, from 0.1 to 2 m, are used for the connection of C_x but did not affect the measured capacitance at all,

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